WHAT IS CLAIMED IS:

1. A method for compiling a design for an integrated circuit, the method comprising:

automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters to generate output values for one or more output metrics;

reporting the output values for the output metrics; and

concluding the compilations when a stopping criteria has been reached.

2. The method according to claim 1 wherein:

the method produces a table of results of the output metrics for each combination of input parameters used for a compilation.

3. The method according to claim 1 wherein:

the method produces a signature of the best configuration of input parameters, for use in future compilations.

4. The method according to claim 1 wherein:

the method produces a metric of average results across a range of input parameters to indicate expected noise or variability.

5. The method according to claim 4 wherein:

the metric is used to distinguish gains due to the input parameters from random fluctuation.

6. The method according to claim 1 wherein:

one of the input parameters is a random seed or initial configuration parameter.

7. The method according to claim 1 wherein:

one of the input parameters is effort level for the compilation tool or a portion of the compilation tool.

8. The method according to claim 1 wherein:

one of the input parameters modifies a default cost of a given resource for placement.

9. The method according to claim 1 wherein:

one of the input parameters modifies a default soft-limit for fitting or synthesis.

10. The method according to claim 1 wherein:

one of the input parameters modifies a coefficient indicating the speed versus resource usage optimization for the compilations.

11. The method according to claim 1 wherein:

one of the input parameters defines a level of effort to a register packing algorithm that combines circuit elements in the design into fewer logic elements on the integrated circuit when enabled.

12. The method according to claim 1 wherein:

one of the input parameters is a balancing parameter to technology mapping in synthesis.

13. The method according to claim 1 wherein:

one of the input parameters adds or deletes one optimization algorithm or step from a default CAD flow, or modifies an order in which CAD steps are applied to the integrated circuit.

14. The method according to claim 1 wherein:

one of the input parameters is a choice or specification of an alternate synthesis optimization script.

15. The method according to claim 1 wherein:

one of the input parameters enables a netlist optimization or physical resynthesis step.

16. The method according to claim 1 wherein:

the set of output metrics include a measure of the longest delay path in the design.

17. The method according to claim 1 wherein:

the set of output metrics includes a quantification of logic area or other resource usage of the integrated circuit.

18. The method according to claim 1 wherein:
the set of output metrics includes an estimate of power consumption.

19. The method according to claim 1 wherein:
the set of output metrics includes a metric for a number of paths, register-register pairs, IO-register pairs, or register-IO pairs that fail to meet a specified timing constraint.

20. The method according to claim 1 wherein:
the set of output metrics includes a minimum slack calculated on the integrated circuit.

21. The method according to claim 1 wherein:
the set of output metrics includes a total slack calculated on the integrated circuit.

22. The method according to claim 1 wherein:
the stopping criteria for the method is based on exhausting all possible combination of specified input parameters independent of results.

23. The method according to claim 1 wherein:
the stopping criteria is based on achieving a user's specified constraints.

24. The method according to claim 1 wherein:
the stopping criteria is a total compile time consumed over all of the compilations thus far.

25. The method according to claim 1 wherein:
the stopping criteria is based on a number of failed constraints in the integrated circuit.

26. The method according to claim 1 wherein:
the stopping criteria for the method is based on the number of failing timing paths in the circuit.

27. The method according to claim 1 wherein:

the stopping criteria is based on achieving a minimum worst-case slack in the integrated circuit.

28. The method according to claim 1 wherein:
the stopping criteria is based on a total slack in the circuit.

29. The method according to claim 1 wherein:
the stopping criteria is based on a statistical calculation of possible success by the method.

30. The method according to claim 1 wherein:
an order of configurations tested is a static schedule pre-calculated by a tool.

31. The method according to claim 1 wherein:
the order of configurations is dynamically modified based on a metric of current distance from the user goals.

32. A computer system for automating compilation of a design for an integrated circuit, the method comprising:
code for automatically performing multiple compilations of the design using a series of values for each input parameter in a set of input parameters to generate output values for one or more output metrics;
code for reporting the output values of the output metrics; and
code for concluding when a stopping criteria has been reached.

33. The computer system according to claim 32 wherein the code for reporting the output values further comprises:
code for producing a table of results of the output metrics for each combination of input parameters used for a compilation.

34. The computer system according to claim 32 further comprising:
code for producing a signature of the best configuration of input parameters, for use in future compilations.

35. The computer system according to claim 32 further comprising:
code for producing a metric of average results across a range of input parameters to indicate expected noise or variability.

36. The computer system according to claim 35 wherein the metric is used to distinguish gains due to the input parameters from random fluctuation.

37. The method according to claim 32 wherein:

one of the input parameters is a random seed or initial configuration parameter.

38. The method according to claim 32 wherein:

one of the input parameters is effort level for the compilation tool or a portion of the compilation tool.

39. The method according to claim 32 wherein:

one of the input parameters modifies a default cost of a given resource for placement.

40. A method for determining tuning parameters for a CAD algorithm or tool, the method comprising:

performing multiple compilations of a design of an integrated circuit using a series of values for each tuning parameter in a set of tuning parameters;

performing multiple compilations of the design using a series of exogenous parameters;

generating outputs values for one or more output metrics;

reporting the output values of the output metrics; and

concluding efficacy of the tuning parameters in the presence of exogenous noise.